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06EC82

Eighth Semester B.E. Degree Examination, June 2012
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is an embedded system? Why is it so hard to define? **(04 Marks)**

b. Define time-to-market and NRE cost matrics? The life time of a product is 58 weeks. If the product is delayed by 5 weeks, determine the percentage revenue loss? Determine the per product cost if NRE cost is Rs.500000.00 and unit cost is Rs.8000.00 and company produces 6000 units of that product. **(08 Marks)**

c. Explain how the top-down design process improves the productivity. **(08 Marks)**

2 a. Explain the purpose of controller and datapath in a single purpose processor. **(04 Marks)**

b. Write a simple algorithm to find GCD of two integer numbers. Write FSMD for this algorithm and explain how it can be optimized. Also write its optimized FSMD. **(08 Marks)**

c. Explain in brief, standard software development process used in embedded system. **(08 Marks)**

3 a. What is watch-dog timer? What is its use? A 16-bit timer operates at a clock frequency of 20 MHz. Determine the resolution and range of this timer. If a ÷ 4 prescalar is also used, what is the range and resolution of this design? **(06 Marks)**

b. Highlight the advantages of using data in digital form over its analog form. Explain the working of successive approximation type of analog to digital converter, with an example. **(10 Marks)**

c. Explain the features of flash memory and DRAM. **(04 Marks)**

4 a. Explain in brief, the memory hierarchy and cache operation. Given the following three cache designs, find the one with the best performance, by calculating the average cost of access.

i) 4 kbytes, 8-way set associative cache with 6% miss rate. Cache hit costs 1-cycle, cache miss costs 12-cycles.

ii) 8 kbytes, 4-way set associative cache with 4% miss rate. Cache hit costs 2-cycles, cache miss costs 12-cycles.

iii) 16 kbytes, 2-way set associative cache with 2% miss rate. Cache hit costs 3-cycles, cache miss costs 12-cycles. **(10 Marks)**

b. Design a 2k×16 ROM using 1k×8 ROM using an address decoder. **(04 Marks)**

c. Write the features of USB and IEEE 802.11 protocol. **(06 Marks)**

PART – B

5 a. With an example, explain shared data problem. Also explain how an interrupt facility can solve this shared data problem. **(10 Marks)**

b. Define interrupt latency. Mention the factors that affects interrupt latency. **(04 Marks)**

c. Explain in brief, Function-Queue-Scheduling architecture. **(06 Marks)**

6 a. Briefly compare the methods for intertask communication. **(10 Marks)**

b. Explain in brief, three different states of task in RTOS. **(05 Marks)**

c. Briefly compare the three methods of protecting shared data. **(05 Marks)**

7 a. What are the two rules, that interrupt routines in most RTOS environment must follow, that do not apply to task codes? **(05 Marks)**

b. Illustrate with suitable examples and explain what happens when each rule of question no.7a is violated. **(15 Marks)**

8 a. With suitable example, explain encapsulating semaphores. **(08 Marks)**

b. Briefly explain any six problems with semaphores. **(07 Marks)**

c. Give the hard real-time scheduling considerations. **(05 Marks)**

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